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Officer size y characteristics and to see, the period	01.0 0.0 10 10 10 10	Application Number	10/645,510-Conf. #8761
TRANSMITTAL		Filing Date	August 22, 2003
FORM		First Named Inventor	Chun-Yen TU
(to be used for all correspondence after initial filing)		Art Unit	2182
		Examiner Name	D. E. Martinez
Total Number of Pages in This Submission 3		Attorney Docket Numb	^{oer} 3313-1022P
ENCLOSURES (Check all that apply)			
Fee Transmittal Form	Drawing(s)		After Allowance Communication to TC
Fee Attached	Licensing-related Papers		Appeal Communication to Board of Appeals and Interferences
X Amendment/Reply	Petition		Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
After Final	Petition to Convert to a Provisional Application		Proprietary Information
Affidavits/declaration(s)	Power of Attorney, Revocation Change of Correspondence Address		Status Letter
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Information Disclosure Statement	CD, Number of CD(s)		
Certified Copy of Priority Document(s)	Landscape Table on CD		
Reply to Missing Parts/ Incomplete Application	Remarks		
Reply to Missing Parts under 37 CFR 1.52 or 1.53			
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Firm Name			
BIRCH, STEWART, KOLASCH & BIRCH, LLP			
Signature / / / / · /			

KM/asc

32,334

October 12, 2005

Printed name

Date



Docket No.: 3313-1022P

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Chun-Yen TU

Application No.: 10/645,510

Confirmation No.: 8761

Filed: August 22, 2003

Art Unit: 2182

For: DATA TRANSMISSION METHOD FOR

MICROPROCESSORS IN A

PROGRAMMABLE LOGIC CONTROLLER

Examiner: D. E. Martinez

REPLY TO RESTRICTION REQUIREMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In reply to the Restriction Requirement dated September 12, 2005, the following remarks are respectfully submitted in connection with the above-identified application.

REMARKS

Claims 1-12 are pending in the present application.

The Examiner has required election in the present application between:

Group I, claim 1, drawn to a connection between a master processor and a slave processor; and

Group II, claims 2-12, drawn to a digital signal format comprised of characters defined by bits.